

1 RECEIVING APPARATUS

FIG. 1

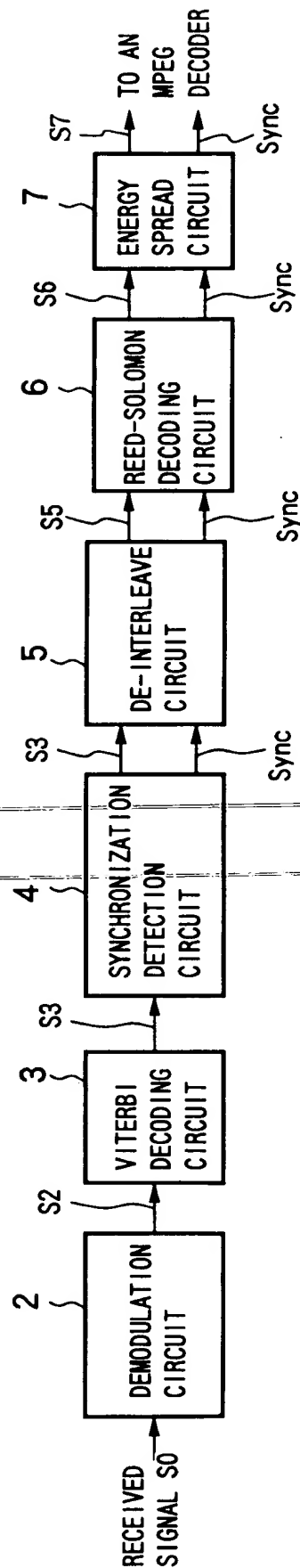
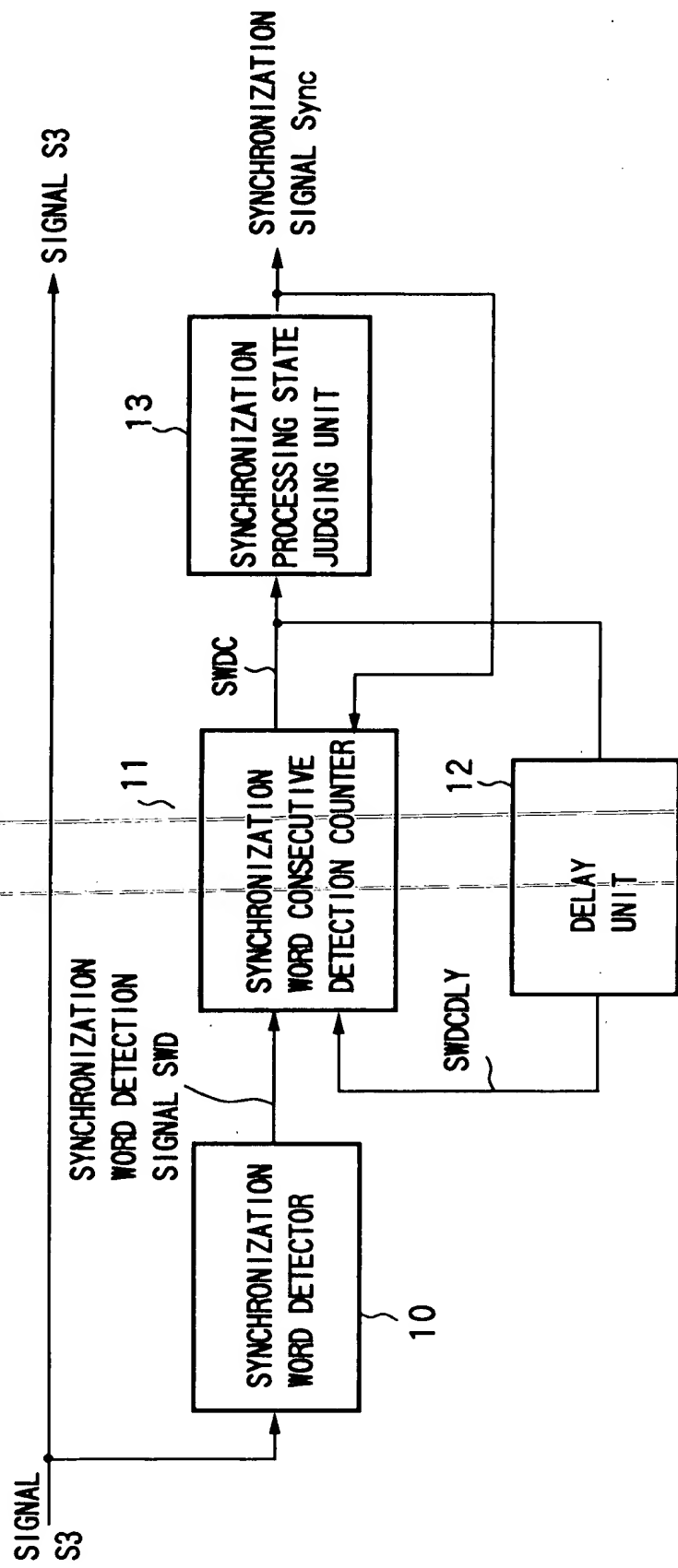
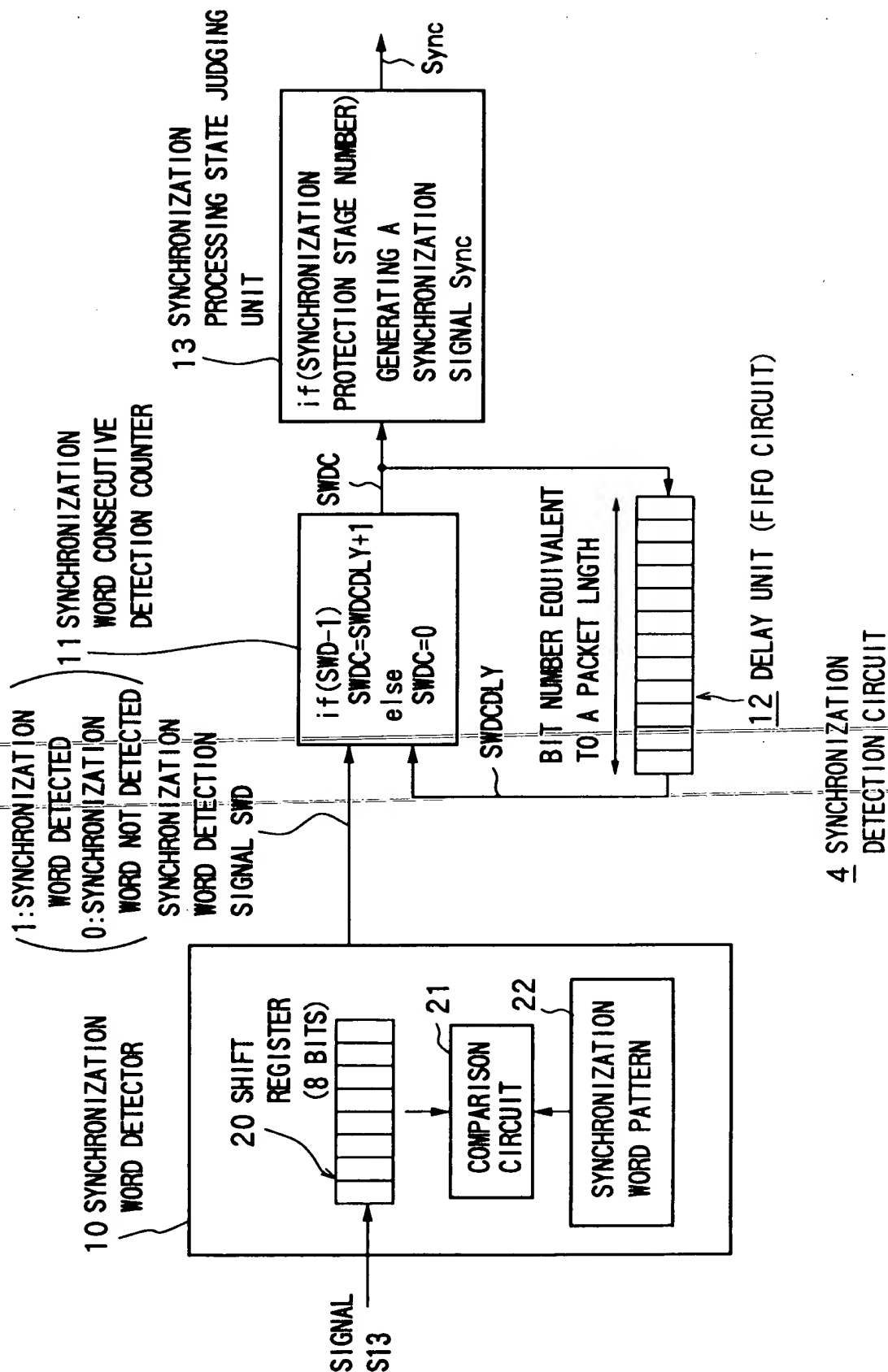


FIG.2



4 SYNCHRONIZATION
DETECTION CIRCUIT

FIG. 3



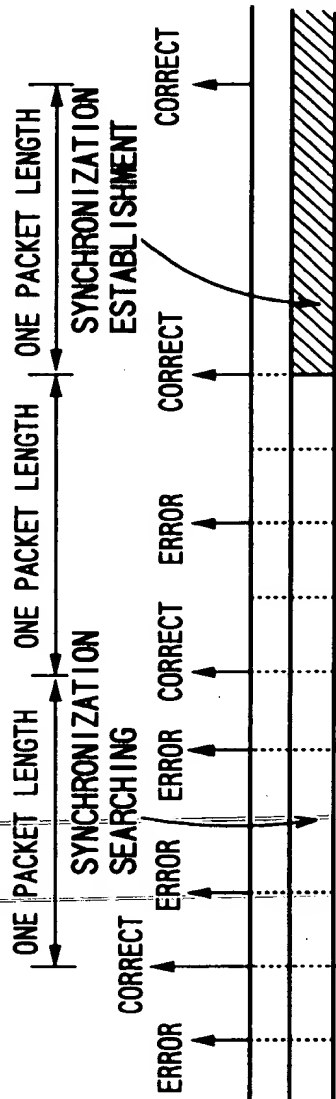


FIG. 4A Synchronization Processing State

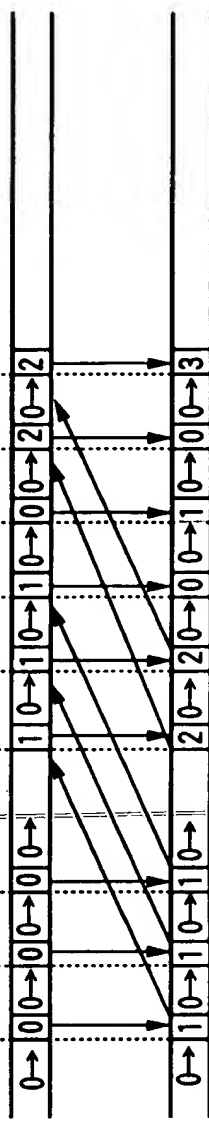


FIG. 4B

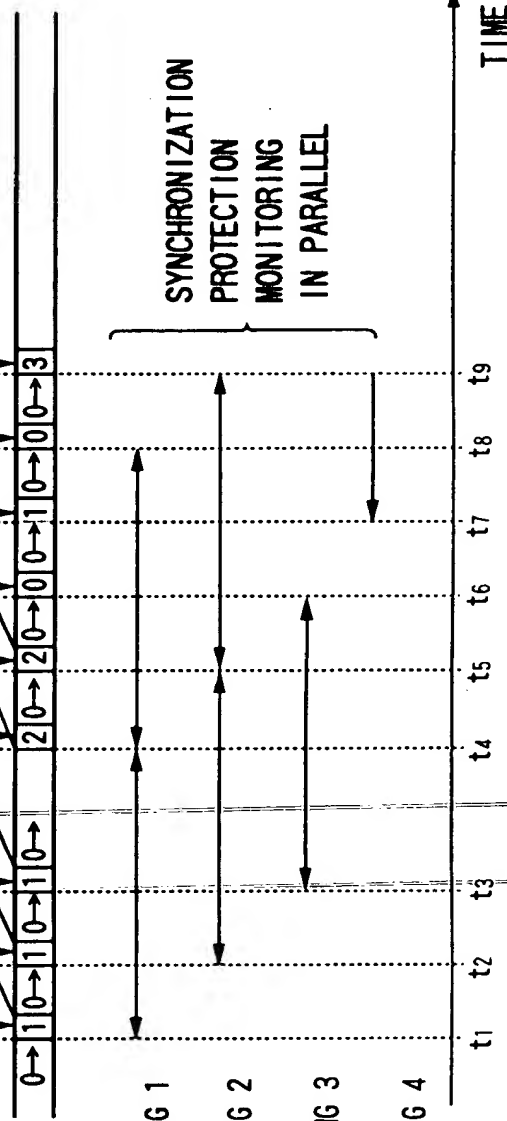


FIG. 4C

FIG. 5

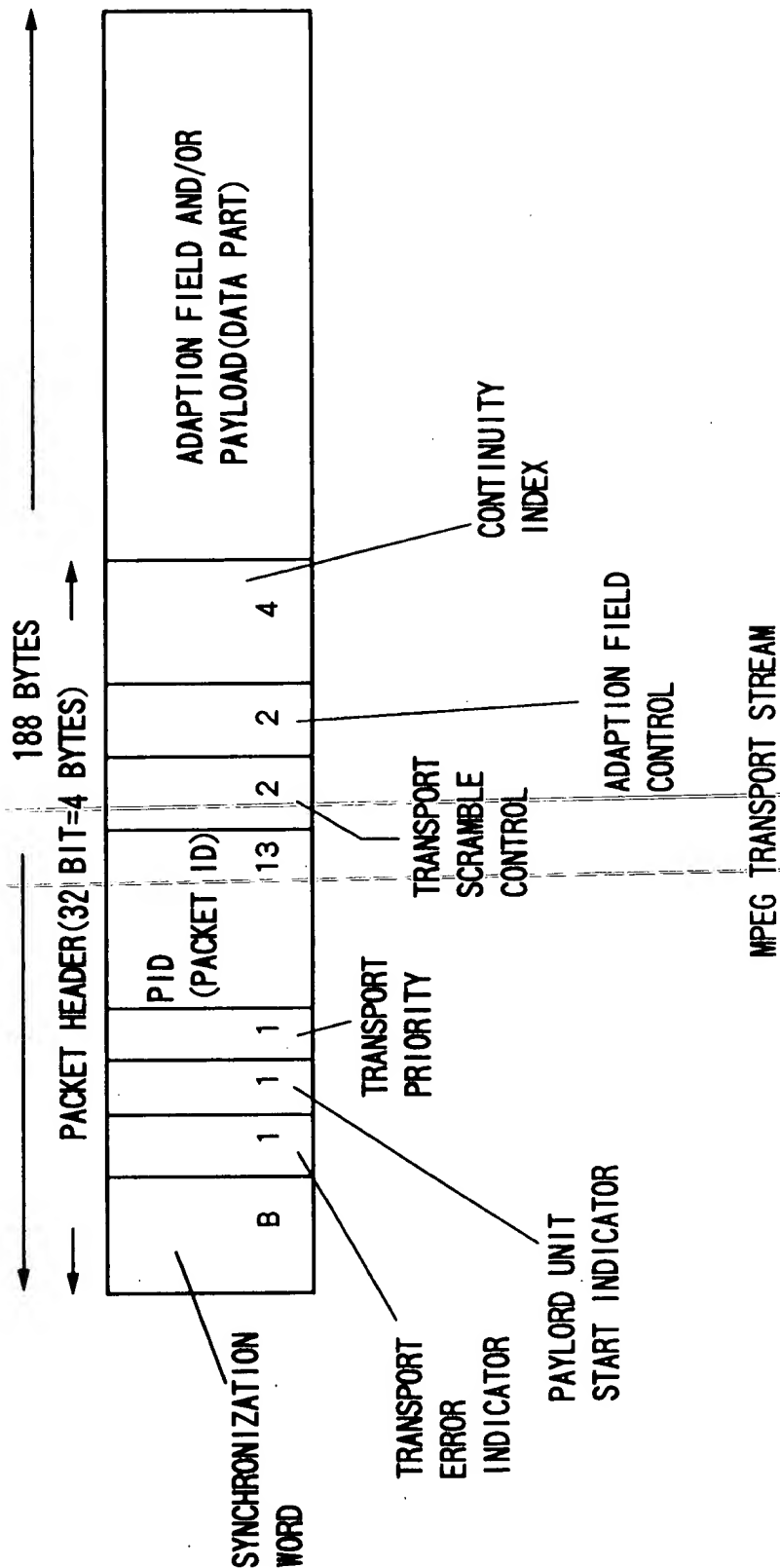


FIG. 6A TRANSPORT
STREAM PACKET

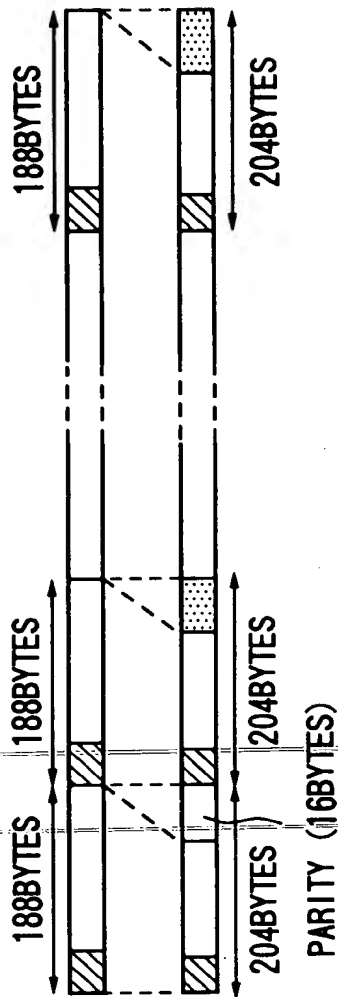


FIG. 6B SLOT DATA



